

Fig. 1

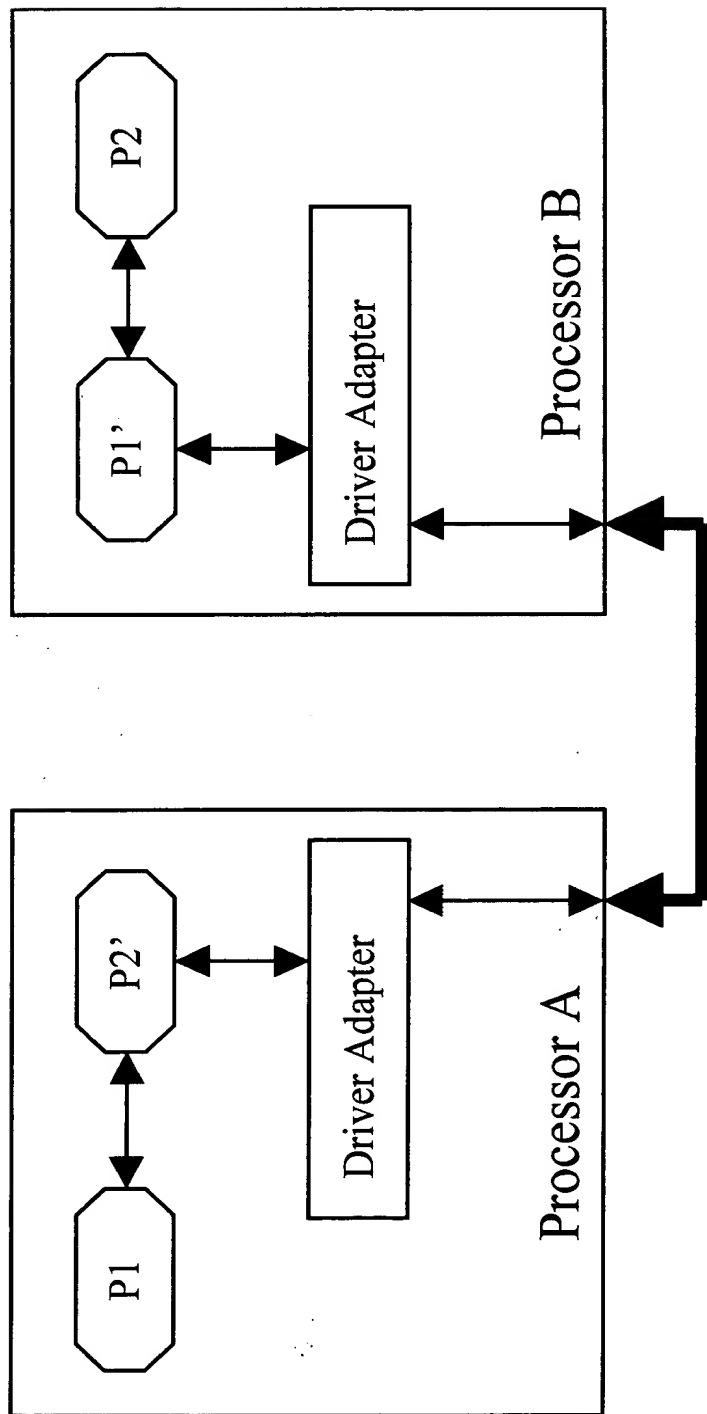


Fig. 2

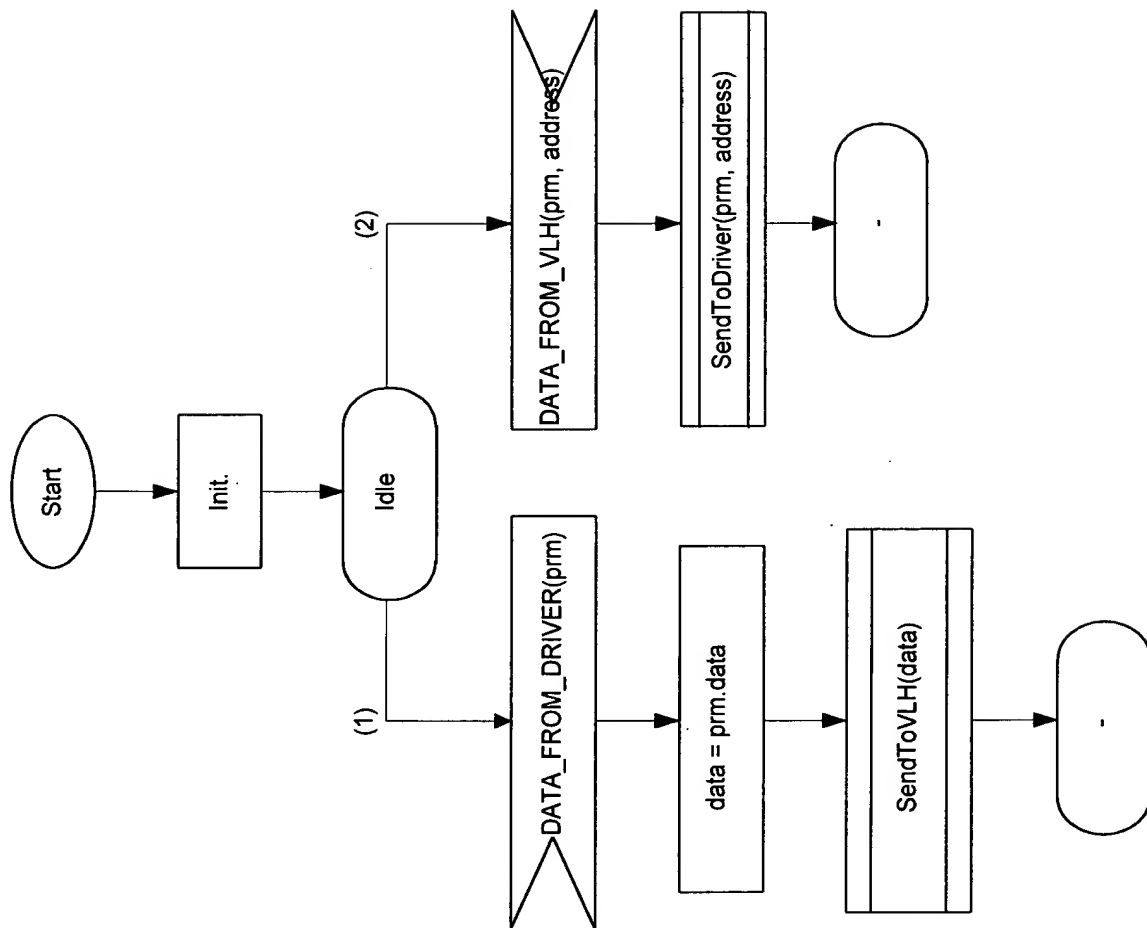


Fig. 3

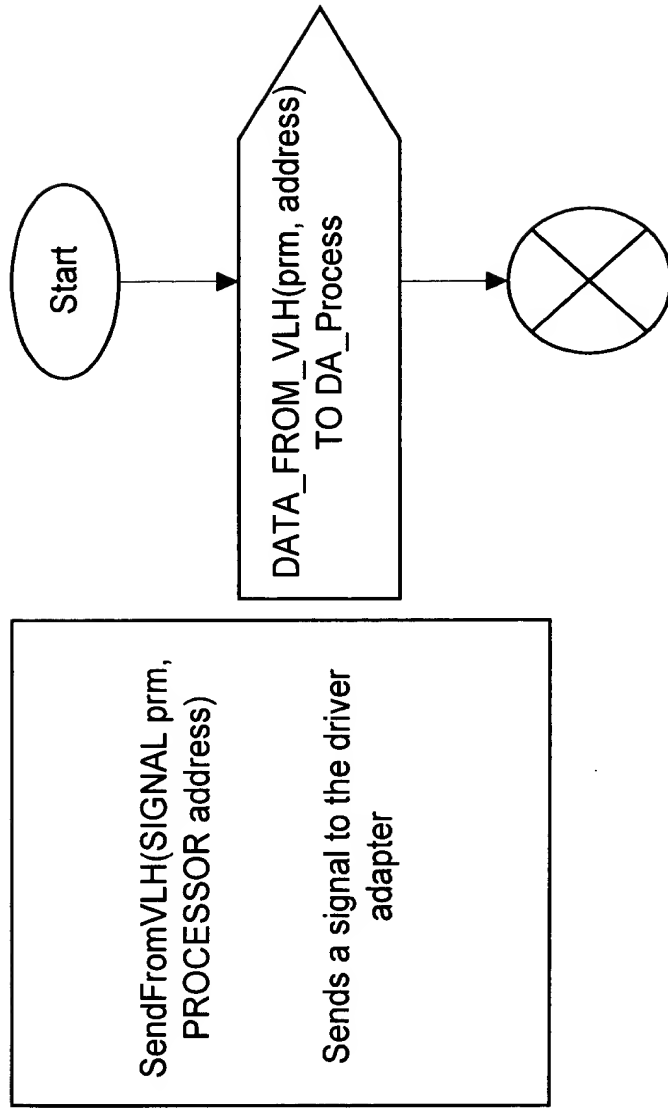


Fig. 4

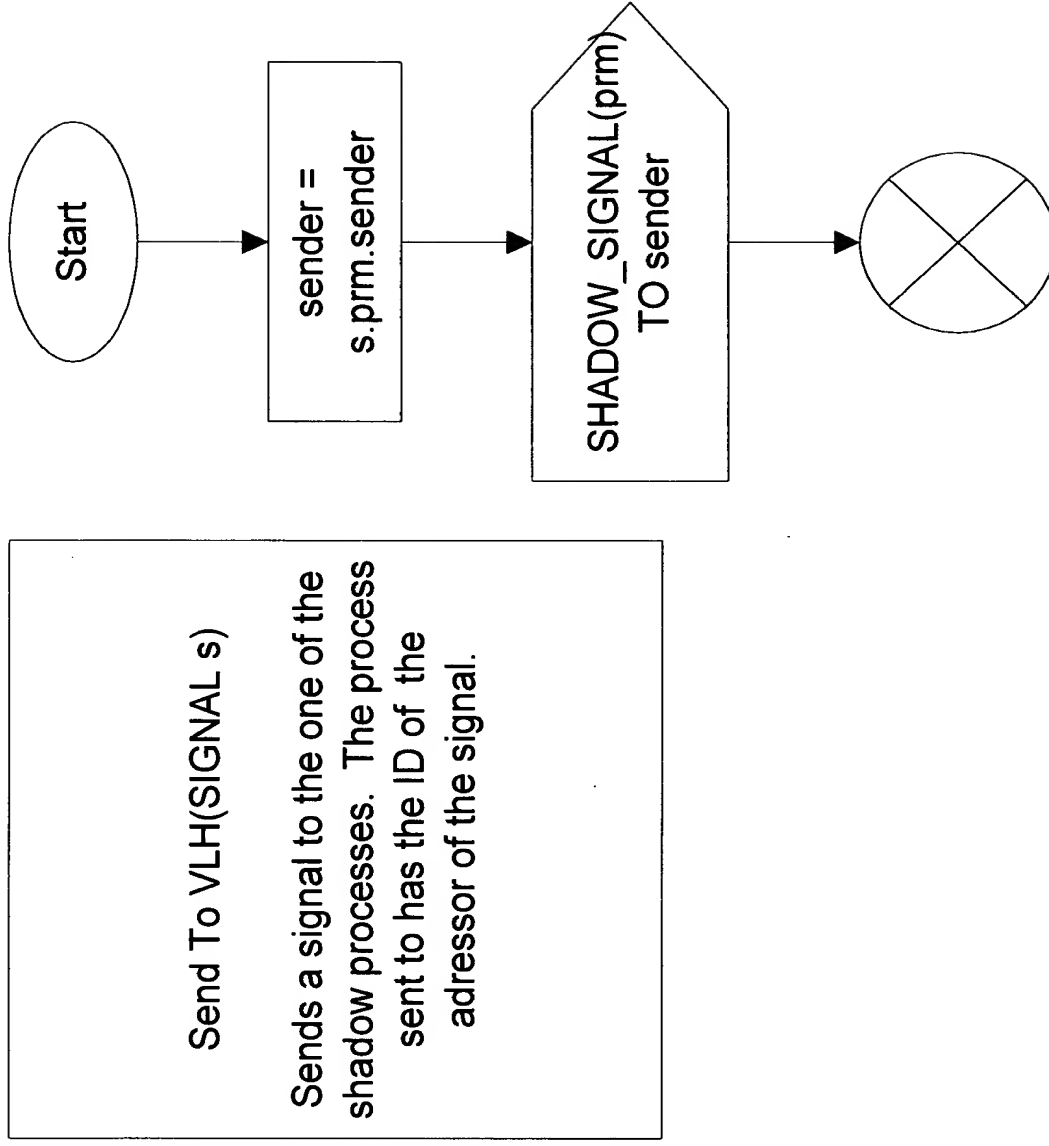
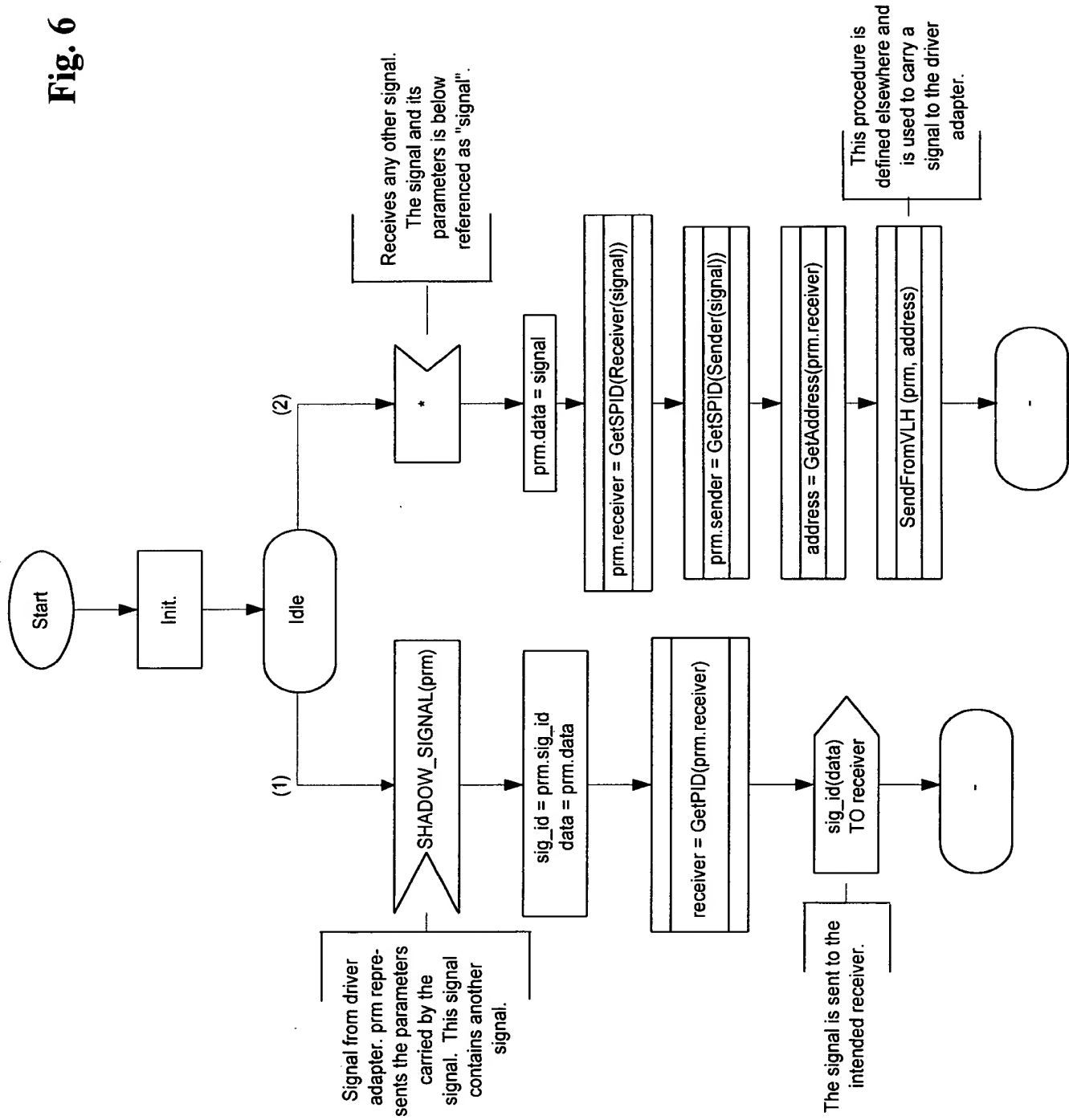


Fig. 5

Fig. 6



Processor A PIDs	Shadow PIDs	Address	Processor B PIDs
P1	sP1	A	P1'
P2	sP2	A	P2'
P3	sP3	A	P3'
P4'	sP4	B	P4
P5'	sP5	B	P5
P6'	sP6	B	P6
-	-	B	P7

Fig. 8

Processor A			Processor B		
PIDs	Shadow PIDs	Address	Address	Shadow PIDs	PIDs
P1	sP1	A	A	sP1	P1'
P2	sP2	A	A	sP2	P2'
P3	sP3	A	A	sP3	P3'
P4'	sP4	B	B	sP4	P4
P5'	sP5	B	B	sP5	P5
P6'	sP6	B	B	sP6	P6
-	-	-	B	-	P7

Fig. 9a

Processor A		
PIDs	Shadow PIDs	Address
P1	sP1	A
P2	sP2	A
P3	sP3	A
P4'	sP4	B
P5'	sP5	B
P6'	sP6	B

Processor B		
Address	Shadow PIDs	PIDs
A	sP1	P1'
A	sP2	P2'
A	sP3	P3'
B	sP4	P4
B	sP5	P5
B	sP6	P6

Fig. 9b

Processor A	
PIDs	Shadow PIDs
P1	sP1
P2	sP2
P3	sP3
P4'	sP4
P5'	sP5
P6'	sP6

Processor B	
Shadow PIDs	PIDs
sP1	P1'
sP2	P2'
sP3	P3'
sP4	P4
sP5	P5
sP6	P6

Fig. 9c

